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James C. Scheller
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,478	BRATT ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004 and 06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-48 and new claims 49-50 have been examined. New claims 49-50 have been added as per Applicant's request. Claims 1, 2, 8, 15, 20, 25, and 39 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as filed 26 November 2004; IDS as filed 26 November 2004; and IDS as filed 06 December 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11-24 and 35-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Barry et al., U.S. Patent No. 6,397,324.

5. Regarding claims 11 and 35, taking claim 11 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Receiving a plurality of numbers (see An/Rz of Fig.6). Here, the L2TBL instruction, which is the LTBL instruction modified to perform two look-up table look-ups (see Col.9 lines 53-62), specifies two base registers (An.H1 and An.H0)

and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (see Col.10 line 62 – Col.11 line 32).

b. Partitioning look-up memory into a plurality of look-up tables (see Col.7 lines 54-62 and Col.9 lines 63-67),

c. Look up simultaneously a plurality of elements from the plurality of look-up tables (431/433 of Fig.4), each of the plurality of elements being in one of the plurality of look-up tables and being pointed to by one of the plurality of numbers (see Col.9 lines 41-67 and Col.12 lines 14-27). Here, the above two pointers received point to elements in the look-up tables, and the L2TBL instruction subsequently reads the elements pointed to and stores them in a corresponding entry in the register file.

d. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "L2TBL" on Col.10 line 62 – Col.11 line 32).

6. Claim 35 is nearly identical to claim 11, differing in its method being comprised upon a machine-readable medium (see Barry, Fig.8A), but encompassing the same scope as claim 11. Therefore, claim 35 is rejected for the same reasons as claim 11.

7. Regarding claims 12 and 36, taking claim 12 as exemplary, Barry has taught a method as in claim 11, wherein the receiving a plurality of numbers comprises:

a. Partitioning a string of bits into a plurality of segments to generate the plurality of numbers (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register, and partitions them into two segments of data, Rze and Rzo based on the even and odd source register address.

8. Claim 36 is nearly idéntical to claim 12, differing in its parent claim, but encompassing the same scope as claim 12. Therefore, claim 36 is rejected for the same reasons as claim 12.

9. Regarding claims 13 and 37, taking claim 13 as exemplary, Barry has taught a method as in claim 12, wherein the single instruction specifies format information in which the plurality of numbers are stored in the string of bits (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Ṙz register (see Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

10. Claim 37 is nearly identical to claim 13, differing in its parent claim, but encompassing the same scope as claim 13. Therefore, claim 37 is rejected for the same reasons as claim 13.

11. Regarding claims 14 and 38, taking claim 14 as exemplary, Barry has taught a method as in claim 11, wherein the look-up memory comprises a plurality of look-up units (431/433 of Fig.4), and wherein said partitioning look-up memory comprises:

a. Configuring the plurality of look-up units into the plurality of look-up tables (see Col.7 lines 54-62 and Col.9 lines 63-67).

12. Claim 38 is nearly identical to claim 14, differing in its parent claim, but encompassing the same scope as claim 14. Therefore, claim 38 is rejected for the same reasons as claim 14.

13. Regarding claims 15 and 39, taking claim 15 as exemplary, Barry has taught a method as in claim 12, wherein the string of bits is received from an entry of a register file (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register (see Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

14. Claim 39 is nearly identical to claim 15, differing in its parent claim, but encompassing the same scope as claim 15. Therefore, claim 39 is rejected for the same reasons as claim 15.

15. Regarding claims 16 and 40, taking claim 16 as exemplary, Barry has taught a method as in claim 15, wherein the single instruction specifies an index of the entry (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies a string of bits within the Rz register (see Fig.6A), and formats them into two segments of data, Rze and Rzo based on the even and odd source register address (see Col.10 line 62 – Col.11 line 32).

16. Claim 40 is nearly identical to claim 16, differing in its parent claim, but encompassing the same scope as claim 16. Therefore, claim 40 is rejected for the same reasons as claim 16.

17. Regarding claims 17 and 41, taking claim 17 as exemplary, Barry has taught a method as in claim 11, further comprising:

a. Storing the plurality of elements in an entry of the register file (see Col.10 line 62 – Col.11 line 32).

18. Claim 41 is nearly identical to claim 17, differing in its parent claim, but encompassing the same scope as claim 17. Therefore, claim 41 is rejected for the same reasons as claim 17.

19. Regarding claims 18 and 42, taking claim 18 as exemplary, Barry has taught a method as in claim 17, wherein the single instruction specifies an index of the entry (see Rt of Fig.6A and Col.10 line 62 – Col.11 line 32).

20. Claim 42 is nearly identical to claim 18, differing in its parent claim, but encompassing the same scope as claim 18. Therefore, claim 42 is rejected for the same reasons as claim 18.

21. Regarding claims 19 and 43, taking claim 19 as exemplary, Barry has taught a method as in claim 17, wherein the single instruction specifies format information in which the plurality of

elements are stored in the entry (see Col.10 line 62 – Col.11 line 32). Here, the L2TBL instruction specifies that the plurality of data entries are stored at even and odd addresses into the register file, thus specifying the format.

22. Claim 43 is nearly identical to claim 19, differing in its parent claim, but encompassing the same scope as claim 19. Therefore, claim 43 is rejected for the same reasons as claim 19.

23. Regarding claims 20 and 44, taking claim 20 as exemplary, Barry has taught a method as in claim 11, the look-up memory comprises a plurality of look-up units, and wherein said partitioning look-up memory comprises: configuring the plurality of look-up units into the plurality of look-up tables (see Col. 10, lines 24-45; Col. 10, line 62 to Col. 11, line 48; and column 11, line 65 to column 12, line 27) wherein each of the plurality of look-up units comprises 256 8-bit entries (see Col.10 line 62 - Col.11 line 48). Here, Barry supports look-up table sizes of 256 (see Col.11 line 44) and 64000 (see Col.11 lines 13-14) entries, each entry being an 8, 16 or 32-bit entry.

24. Claim 44 is nearly identical to claim 20, differing in its parent claim, but encompassing the same scope as claim 20. Therefore, claim 44 is rejected for the same reasons as claim 20.

25. Regarding claims 21 and 45, taking claim 21 as exemplary, Barry has taught a method as in claim 11, wherein the single instruction specifies a total number of entries contained in each of the plurality of look-up tables (see Col.10 line 62 - Col.11 line 48). Here, Barry supports three instructions (STBL, S2TBL and S4TBL) that each specify a different number of entries in the look-up tables, as well as the size of each entry.

26. Claim 45 is nearly identical to claim 21, differing in its parent claim, but encompassing the same scope as claim 21. Therefore, claim 45 is rejected for the same reasons as claim 21.

27. Regarding claims 22 and 46, taking claim 22 as exemplary, Barry has taught a method as in claim 21, wherein the total number of entries is one of:

a. 256 (see Col.11 line 44),

b. 512

c. 1024.

28. Here, Barry supports look-up table sizes of 256 (see Col.11 line 44) and 64000 (see Col.11 lines 13-14) entries, each entry being an 8, 16 or 32-bit entry. Because the claim has been written in the alternative format, only one of the alternative limitations is required to be taught by the prior art, and thus Barry has taught the limitations of claim 22.

29. Claim 46 is nearly identical to claim 22, differing in its parent claim, but encompassing the same scope as claim 22. Therefore, claim 46 is rejected for the same reasons as claim 22.

30. Regarding claims 23 and 47, taking claim 23 as exemplary, Barry has taught a method as in claim 11, wherein the single instruction specifies a total number of bits used by each entry contained in the plurality of look-up tables (see Col.12 lines 14-28). Here, the "size" field of the S2TBL instruction (see Fig.8A and Col.12 lines 66-67) specifies whether the instruction is to use dual word, word, dual-half word or dual byte data is used in the look-up table entries (see Col.10 line 62-Col.11 lines 27 and Col.12 lines 14-28).

31. Claim 47 is nearly identical to claim 23, differing in its parent claim, but encompassing the same scope as claim 23. Therefore, claim 47 is rejected for the same reasons as claim 23.

32. Regarding claims 24 and 48, taking claim 24 as exemplary, Barry has taught a method as in claim 21, wherein the total number of bits is one of:

a. 8 ("two bytes" in Col.12 lines 14-28),

b. 16 ("two halfwords" in Col.12 lines 14-28),

c. 24.

33. Because the claim has been written in the alternative format, only one of the alternative limitations is required to be taught by the prior art, and thus Barry has taught the limitations of claim 24.

34. Claim 48 is nearly identical to claim 24, differing in its parent claim, but encompassing the same scope as claim 24. Therefore, claim 48 is rejected for the same reasons as claim 24.

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 1-10, 25-24, and 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barry et al., U.S. Patent No. 6,397,324 (herein referred to as Barry) in view of Priem, U.S. Patent Number 5,768,628 (herein referred to as Priem).

37. Regarding claims 1 and 25, taking claim 1 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction (Barry "S2TBL" on Col.12 lines 13-27), the method comprising:

a. Receiving a first plurality of numbers (Barry An/Ri of Fig.4 or An/Rz of Fig.8) and a second plurality of numbers (Barry Rs of Fig.4 or Rte/Rto of Fig.8), each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables (Barry 431/433 of

Fig.4) (Barry Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores (Barry Col.9 lines 53-62), specifies two base registers (Barry An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (Barry Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (Barry Col.10 lines 5-20).

b. Replacing simultaneously the plurality of entries in the plurality of look-up tables with the second plurality of numbers (Barry Col.9 lines 41-62 and Col.12 lines 14-27),

c. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Barry "S2TBL" on Col.12 lines 13-27).

38. Barry has not taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit. Priem has taught wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improves processor speed and efficiency.

39. Claim 25 is nearly identical to claim 1, differing in its method being comprised upon a machine-readable medium (Barry, Fig.8A), but encompassing the same scope as claim 1. Therefore, claim 25 is rejected for the same reasons as claim 1.

40. Regarding claims 2 and 26, taking claim 2 as exemplary, Barry has taught a method as in claim 1, wherein:

a. The first plurality of numbers are received from a first entry in a register file (Barry Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction specifies, using even/odd addressing, two base registers (Barry An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (Barry Col.12 lines 14-27). Thus, the execution unit "receives" the first plurality of numbers from a first entry in a register file (Barry An + Rz).

b. The second plurality of numbers are received from a second entry in the register file (Barry Col.9 line 25 – Col.10 line 20 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction specifies two pieces of data denoted by odd and even addresses (each data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (Barry Col.10 lines 5-20).

41. Claim 26 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope as claim 2. Therefore, claim 26 is rejected for the same reasons as claim 2.

42. Regarding claims 3 and 27, taking claim 3 as exemplary, Barry has taught a method as in claim 2, wherein the single instruction specifies indices of the first (Barry An and Rz of Fig.8, Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27) and second entries (Barry Rt in Fig:8, Col.9 line 25 – Col.10 line 20 and Col.11 line 64 – Col.12 line 27) in the register file.

43. Claim 27 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope as claim 3. Therefore, claim 27 is rejected for the same reasons as claim 3.

44. Regarding claims 4 and 28, taking claim 4 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Replacing at least one entry in at least one of a plurality of look-up units (Barry 431/433 of Fig.4) in a microprocessor unit with at least one number (Barry Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores (see Col.9 lines 53-62), specifies two base registers (Barry An.H1 and An.H0) and two offsets (Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (Barry Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers

created (Barry Col.10 lines 5-20). The entries are updated via the memory interface unit (Barry 485 of Fig.4).

b. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (see "S2TBL" on Col.12 lines 13-27).

45. Barry has not taught using a Direct Memory Access (DMA) controller. Priem has taught using a Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improves processor speed and efficiency.

46. Claim 28 is nearly identical to claim 4, differing in its parent claim, but encompassing the same scope as claim 4. Therefore, claim 28 is rejected for the same reasons as claim 4.

47. Regarding claims 5 and 29, taking claim 5 as exemplary, Barry has taught a method for execution by a microprocessor in response to receiving a single instruction, the method comprising:

a. Replacing at least one entry for each of a plurality of look-up units (Barry 431/433 of Fig.4) in a microprocessor with a plurality of numbers (Barry Col.9 lines 25-52 and Col.11 line 64 – Col.12 line 27). Here, the S2TBL instruction, which is the STBL instruction modified to perform two look-up table stores

(Barry Col.9 lines 53-62), specifies two base registers (Barry An.H1 and An.H0) and two offsets (Barry Rze and Rzo) to create two pointers (a plurality of "numbers") to an entry in one of the look-up tables (Barry Col.12 lines 14-27). The S2TBL instruction further specifies two pieces of data denoted by even and odd addresses (each piece of data is considered a number) stored in the register file at Rte and Rto that will be written into the look-up table entries pointed to by the pointers created (Barry Col.10 lines 5-20). The entries are updated via the memory interface unit (Barry 485 of Fig.4).

b. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Barry "S2TBL" on Col.12 lines 13-27).

48. Barry has not taught using a Direct Memory Access (DMA) controller. Priem has taught using a Direct Memory Access (DMA) controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improves processor speed and efficiency.

49. Claim 29 is nearly identical to claim 5, differing in its method being comprised upon a machine-readable medium (Barry, Fig.8A), but encompassing the same scope as claim 5. Therefore, claim 29 is rejected for the same reasons as claim 5.

50. Regarding claims 6-10 and 30-34, Barry has not taught

a. Taking claim 6 as exemplary, a method as in claim 5, wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units (Applicant's claim 6);

b. Taking claim 7 as exemplary, a method as in claim 5, wherein a single index encoded in the instruction specifies a total number of the at least one entry for each of a plurality of look-up units (Applicant's claim 7);

c. Taking claim 8 as exemplary, a method as in claim 5, wherein a source address of the plurality of numbers is specified in an entry of a register file (Applicant's claim 8);

d. Taking claim 9 as exemplary, a method as in claim 8, wherein the single instruction specifies an index of the entry in the register file (Applicant's claim 9);

e. Taking claim 10 as exemplary, a method as in claim 5, wherein an identity number encoded in the single instruction specifies the DMA controller (Applicant's claim 10);

f. A method as in claim 5, wherein the at least one entry for each of the plurality of look-up units comprises a plurality of entries for each of the plurality of look-up units (Applicant's claim 49); and

g. A method as in claim 11 wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Applicant's claim 50).

51. Priem has taught

a. A method as in claim 5, wherein a single index encoded in the instruction specifies a location of the at least one entry in the plurality of look-up units (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4);

b. A method as in claim 5, wherein a single index encoded in the instruction specifies a total number of the at least one entry for each of a plurality of look-up units (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4);

c. A method as in claim 5, wherein a source address of the plurality of numbers is specified in an entry of a register file (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4);

d. A method as in claim 8, wherein the single instruction specifies an index of the entry in the register file (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

e. A method as in claim 5, wherein an identity number encoded in the single instruction specifies the DMA controller (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4);

f. A method as in claim 5, wherein the at least one entry for each of the plurality of look-up units comprises a plurality of entries for each of the plurality of look-up units (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4); and

g. A method as in claim 11 wherein the microprocessor comprises a media processor integrated with a memory controller for host memory on a single integrated circuit (Priem Abstract; column 6, line 45 to column 7, line 35; column 7, line 56 to column 8, line 4; Figure 3; and Figure 4).

52. In regards to Priem, the DMA controller includes addresses of the data to be copied and a quantity which represents the amount data to be transferred (Priem column 7, lines 1-8), since it needs to know exactly how much data to copy into the look-up tables. A person of ordinary skill in the art at the time the invention was made would have recognized that the memory controller allows data transfers to occur as quickly as possible (Priem column 6, lines 52-54), thereby increasing processor speed and efficiency (Priem column 2, line 64 to column 3, line 5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory controller of Priem in the device of Barry to improves processor speed and efficiency.

53. Claim 30 is nearly identical to claim 6, differing in its parent claim, but encompassing the same scope as claim 6. Therefore, claim 30 is rejected for the same reasons as claim 6. Claim 31 is nearly identical to claim 7, differing in its parent claim, but encompassing the same scope as claim 7. Therefore, claim 31 is rejected for the same reasons as claim 7. Claim 32 is nearly identical to claim 8, differing in its parent claim, but encompassing the same scope as claim 8. Therefore, claim 32 is rejected for the same reasons as claim 8. Claim 33 is nearly identical to claim 9, differing in its parent claim, but encompassing the same scope as claim 9. Therefore, claim 33 is rejected for the same reasons as claim 9. Claim 34 is nearly identical to claim 10,

differing in its parent claim, but encompassing the same scope as claim 10. Therefore, claim 34 is rejected for the same reasons as claim 10.

Response to Arguments

54. Applicant's arguments with respect to claims 1-3, 25-27, and 49-50 have been considered but are moot in view of the new ground(s) of rejection.

55. Applicant's arguments, see Amendment, filed 26 November 2004, with respect to the rejection(s)of claim(s) 4-10 and 28-34 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the above rejection.

56. Applicant's arguments filed 20 November 2004 in regards to claims 11 and 14 have been fully considered but they are not persuasive. Applicant's argue in essence on page 16-18

> Since the look-up tables in the multiple bank memory of Barry are imaginary, based on how one interprets the meaning of the base addresses and offsets, the processor of Barry does not perform "partitioning look-up memory into a plurality of look-up tables,...wherein the above operations are performed in response to the microprocessor receiving the single instruction".

57. This has not been found persuasive. There is nothing in the claim to discount whether the multiple bank memories are imaginary or not. The description from Barry on column 10, lines 24-45; column 10, line 62 to column 11, line 48; and column 11, line 65 to column 12, line 27 describes how the memory is separated into multiple "imaginary" banks, i.e. partitioned into look-up memory, that holds the data for a particular table, i.e. a particular table from a plurality

of tables. The instructions described perform operations on these tables when a single instruction is received.

Conclusion

58. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Priem, U.S. Patent Number 5,968,148, has taught a DMA controller that loads and stores table information to and from main memory to local memory.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

60. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

61. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
4 February 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100